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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/532,991 | 04/28/2005 | Mitsuhiro Yuasa | 101249-56268US | 2959 |

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| EXAMINER | |
|---|---|
| AHMADI, MOHSEN | |
| **ART UNIT** | **PAPER NUMBER** |
| 2812 | |

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H/A

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/532,991 | YUASA, MITSUHIRO | |
| | Examiner | Art Unit | |
| | Mohsen Ahmadi | 2812 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 04/28/2005 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 04/28/2005.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

The application number 10/532991 for a "Process Monitor and System For Producing Semiconductor" field Nov 31, 2002 has been examined.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

**Claims 1-4 and 6-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Roche et al. (US Pat. 2004/0007326).**

**Regarding claim 1**, Figure 3 and 4, of Roche et al. shows a process monitor for monitoring a process using the sensors which are formed on a

semiconductor wafer 14, comprising a capacitor 74, on the sensor as a power supply (See pages. 2 and 3 paragraph [0037-0038]).

**Regarding claim 2**, Roche et al. discloses a memory (microprocessor) 64, to store measured data obtained by the monitoring (See page. 4, paragraph [0039]).

**Regarding claim 3**, Figure 4, of Roche et al. shows a timer (clock) 68, which is used to specify a measuring time and a measuring period (See page. 4, paragraph [0039]).

**Regarding claim 4**, Roche et al. discloses an additional memory 66, for storing the information (See page. 4, paragraph [0039]).

**Regarding claim 6**, Roche et al. discloses a semiconductor manufacturing apparatus having the process monitor, comprising a process monitor housing unit (package) 58, to store process monitor (See pages. 3 and 4, paragraphs [0037-0038]).

**Regarding claim 7**, Roche et al. discloses a semiconductor manufacturing apparatus having the process monitor, comprising a charging unit to charge capacitor, which is the power supply of the process monitor (See pages. 4, paragraph [0039]) also (See page. 6, paragraph [0048]).

**Regarding claim 8**, Roche et al. discloses a semiconductor manufacturing apparatus having the process monitor, comprising a reader/writer which can be a central microprocessor 64, to read and write the measured data stored in memory (See page. 2, paragraph [0010]) also (See pages. 3 and 4, paragraphs [0037-0038]).

**Regarding claim 9**, Roche et al. discloses a semiconductor manufacturing apparatus, comprising a control unit, which compares the measured data read by reader/writer with predetermined reference data and controls the manufacturing process (See pages. 4, paragraph [0039]).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Roche et al. (US Pat. 2004/0007326) in view of Moradi et al. (US Pat. 6,607,965).**

**Regarding claim 5**, Roche et al. discloses all of the claimed features as stated above except for forming a capacitor by stacking a poly-silicon layer and a silicon nitride layer on semiconductor wafer.

Moradi et al. discloses a method of forming a dielectric materials and a method of forming a capacitor.

Moradi et al. discloses a method of forming a capacitor by stacking a poly-silicon layer and a silicon nitride layer on semiconductor wafer (See col. 5, lines 58-67).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the silicon nitride and poly-silicon as disclosed by Moradi et al. in the process of Roche et al. for it's known benefit of forming a capacitor on semiconductor wafer.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsen Ahmadi whose telephone number is 1-571-272-5062. The examiner can normally be reached on Mon-Fri 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 1-571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MA
02/17/2006

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER